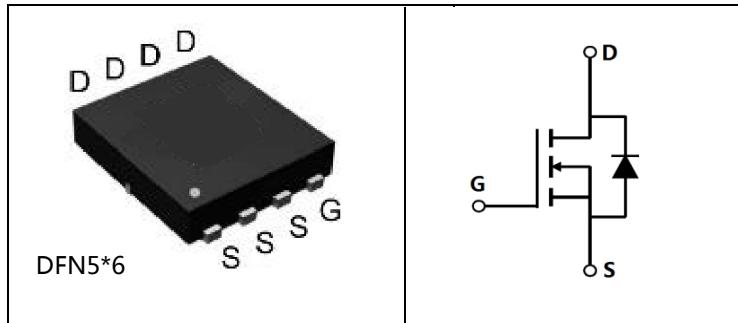


Features

- $BV_{DSS} = 80V$, $I_D = 130A$
- $R_{DS(on)} : 2.6m\Omega$ (typ) @ $V_{GS}=10V$
- N-Channel
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche test



Device Marking and Package Information

Ordering code	Package	Marking
MPGJ80R040	DFN5*6	MPGJ80R040

Maximum ratings, at $T_A = 25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	80	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ C$	A
I_D	Continuous drain current @ $V_{GS}=10V$	$T_C = 25^\circ C$	A
		$T_C = 100^\circ C$	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ C$	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ C$	A
		$T_A = 70^\circ C$	A
EAS	Avalanche energy, single pulsed ②	550	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ C$	W
T_{STG}, T_J	Storage and Junction Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.96	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	63	°C/W



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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=125^\circ\text{C}$)	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=0\text{V}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS(TH)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2.0	--	4.0	V
$R_{\text{DS(ON)}}$	Drain-Source On- State Resistance ③	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=50\text{A}$	--	2.7	4.0	$\text{m}\Omega$

Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, f=100\text{kHz}$	--	5581	--	pF
C_{oss}	Output Capacitance		--	1691	--	pF
C_{rss}	Reverse Transfer Capacitance		--	97.2	--	pF
R_g	Gate Resistance	f=1MHz	--	2	--	Ω
Q_g	Total Gate Charge	$V_{\text{DS}}=40\text{V}, I_{\text{D}}=50\text{A}, V_{\text{GS}}=10\text{V}$	--	61.4	--	nC
Q_{gs}	Gate-Source Charge		--	20	--	nC
Q_{gd}	Gate-Drain Charge		--	8	--	nC

Switching Characteristics

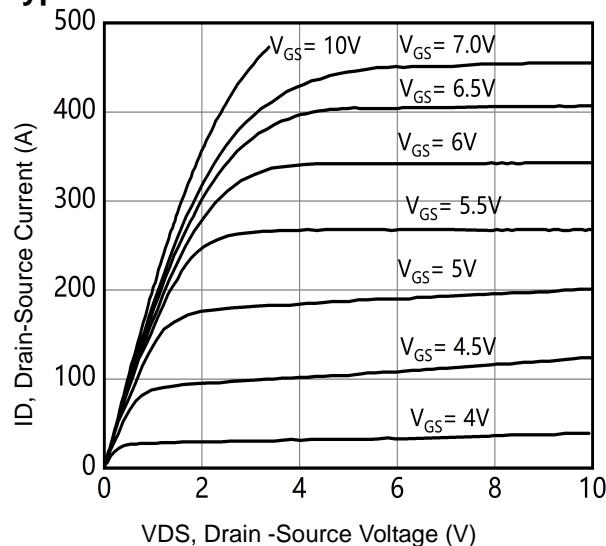
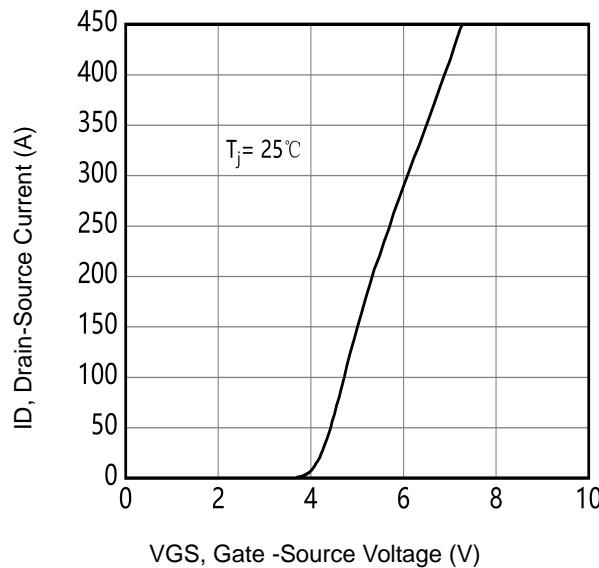
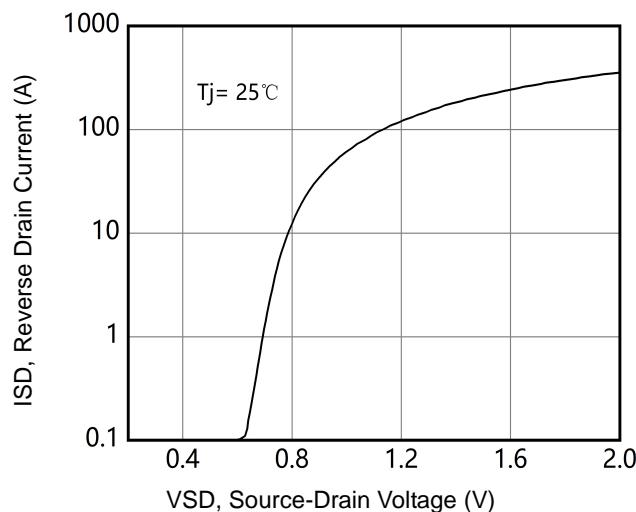
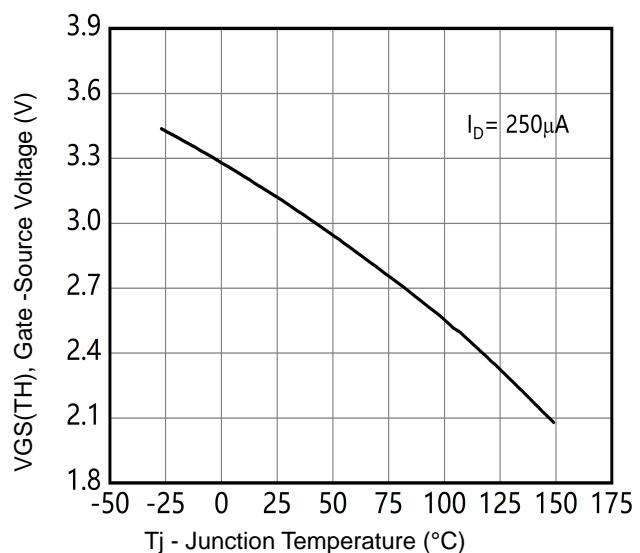
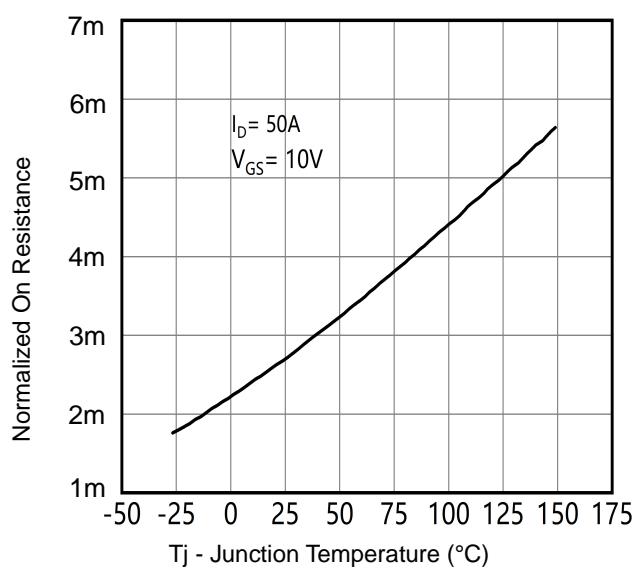
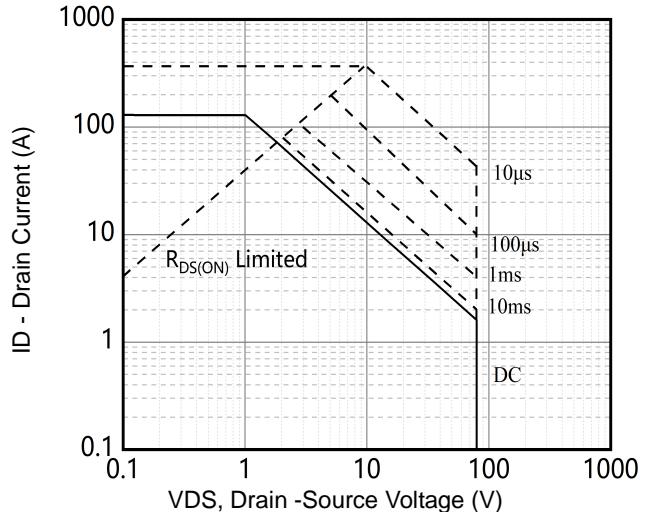
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=40\text{V}, I_{\text{D}}=50\text{A}, R_g=2\Omega, V_{\text{GS}}=10\text{V}$	--	28.5	--	ns
t_r	Turn-on Rise Time		--	10.2	--	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	60	--	ns
t_f	Turn-Off Fall Time		--	15	--	ns

Source- Drain Diode Characteristics@ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

V_{SD}	Forward on voltage	$I_{\text{SD}}=20\text{A}, V_{\text{GS}}=0\text{V}$	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_{\text{SD}}=50\text{A}, V_{\text{GS}}=0\text{V}$	--	65	--	ns
Q_{rr}	Reverse Recovery Charge		--	82	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by $T_{j\text{max}}$, starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_g = 25\Omega$, $I_{\text{AS}} = 10\text{A}$, $V_{\text{GS}} = 10\text{V}$. Part not recommended for use above this value
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

Typical Characteristics

Fig1. Typical Output Characteristics

Fig3. Typical Transfer Characteristics

Fig5. Typical Source-Drain Diode Forward Voltage

Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig4. Normalized On-Resistance Vs. T_j

Fig6. Maximum Safe Operating Area

Typical Characteristics

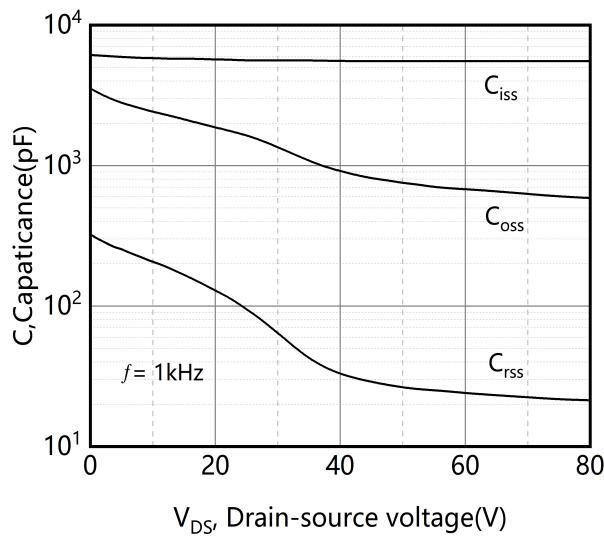


Fig7. Typical Capacitance Vs.Drain-Source Voltage

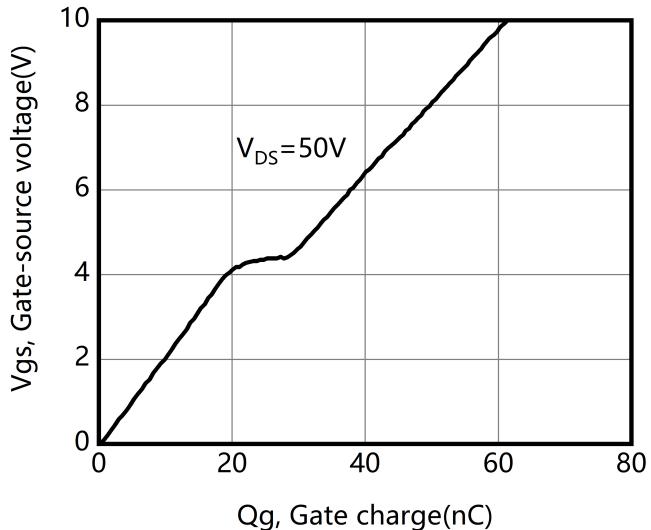


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

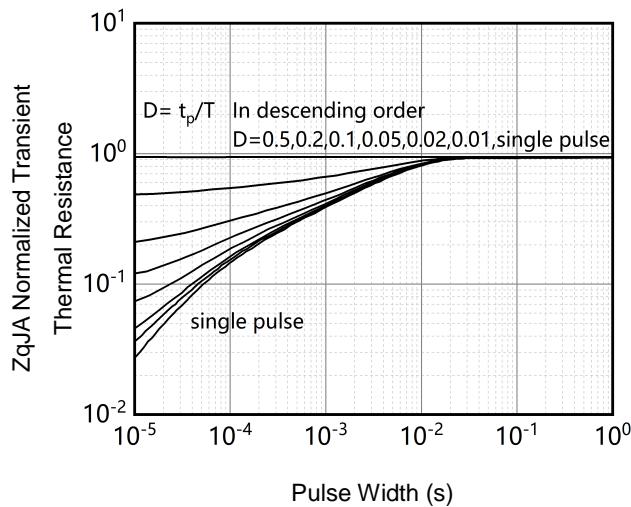
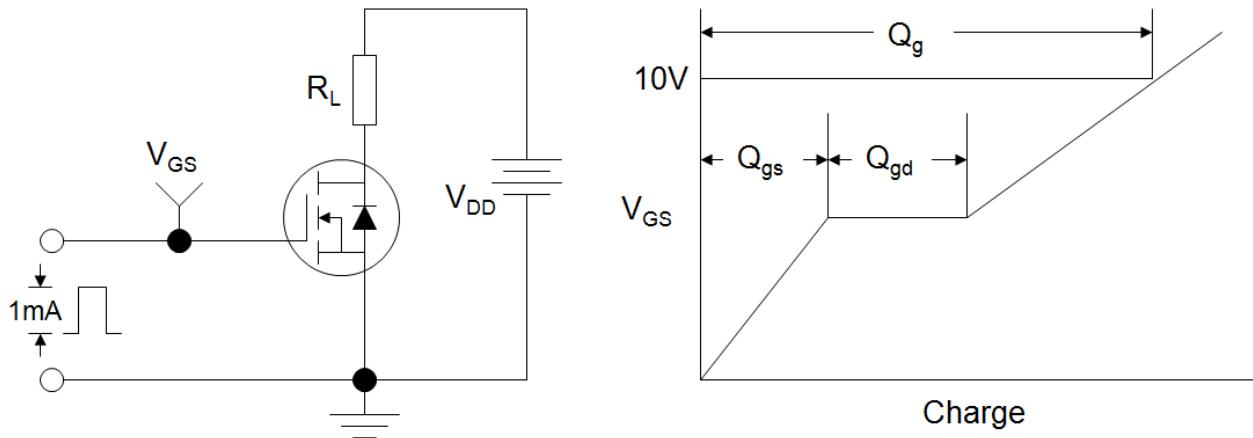
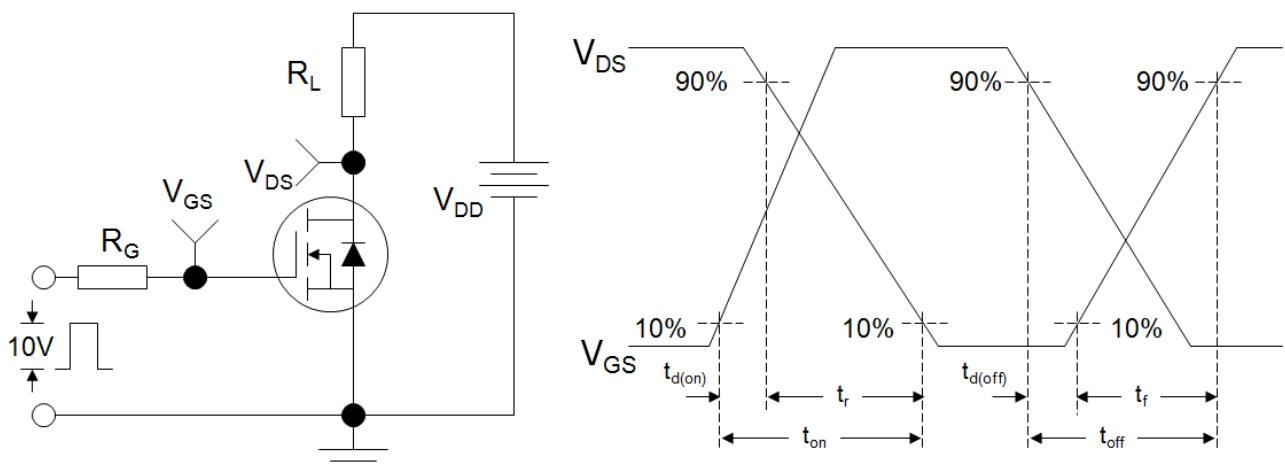
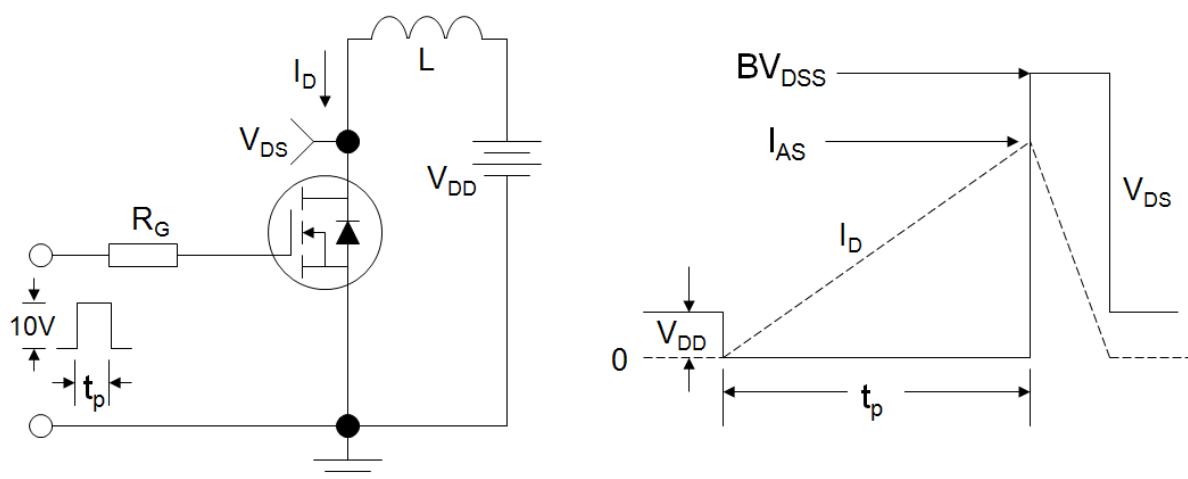
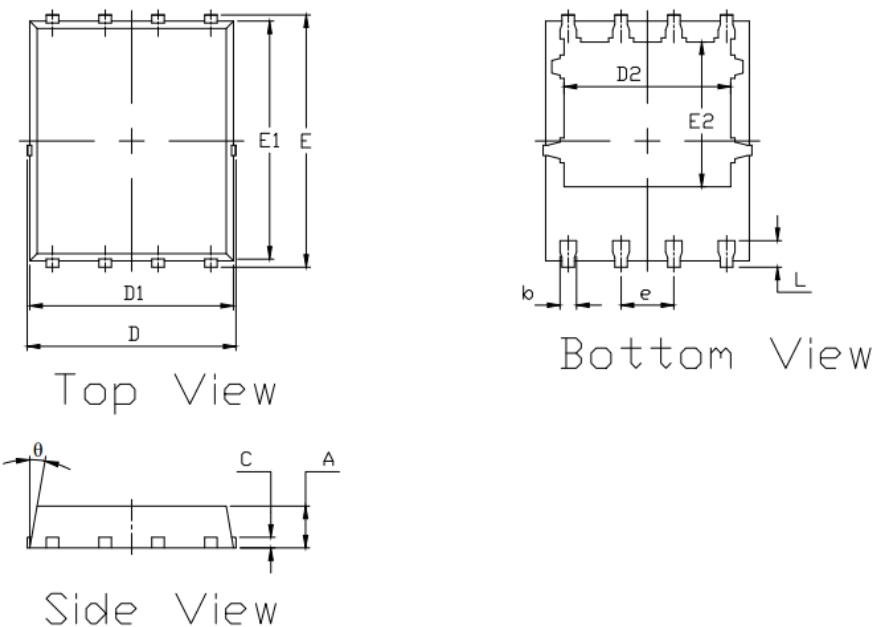


Fig9. Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


Package Information

DFN5*6 package outline dimension



Power56			
DIM.	MIN.	MAX.	TYP.
A	0.95	1.05	1.00
b	0.30	0.50	0.40
C	0.254		
D	5.02		
D1	4.80	5.00	4.90
D2	3.91	4.11	4.01
E	5.95	6.15	6.05
E1	5.60	5.90	5.75
E2	3.38	3.58	3.48
e	1.27REF		
L	0.45	0.65	0.55
θ	10°		



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Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2022-07	Initial version